PIC16C774

PIC16C774 Rev. B Silicon Errata Sheet

The PIC16C774 (Rev. B) parts you have received conform functionally to the Device Data Sheet (DS30275**A**), except for the anomalies described below.

All of the problems listed here will be addressed in future revisions of the PIC16C774 silicon.

1. Module: VREF

If the VRH high voltage reference is enabled and also used as a reference source for the A/D converter, the VRHOEN bit (REFCON<5>) must be set. Since setting the VRHOEN bit connects the VRH reference to the RA3 pin, the TRISA<3> bit must be maintained set and the pin cannot be used for general purpose I/O.

The VRL low voltage reference does not function properly on parts with date codes earlier than 0012NNN, where the first two digits are the year and the second two are the work week. Laser marked parts are made after this date and have a functional VRL. In parts without functional VRL, the VRLEN (REFCON<6>) and VRLOEN (REFCON<4>) bits should be maintained cleared.

Work around

None.

2. Module: PORTE

The minimum VIH specification for PORTE (parameter D040) is 2.2 volts. The maximum VIL specification for PORTE (parameter D030A) is 0.6 volts.

Work around

None.

3. Module: BOR

The Brown-out Reset module's selection ranges have changed. Table 1 shows the new specifications.

Work around

None.

Date Codes Pertaining To This Issue:

All.

Note: When the manufacture date of a newer version of silicon is in production, the last date where this issue may occur will be specified.

TABLE 1: DC SPECIFICATION CHANGES FROM DATA SHEET

Param No.	Sym.	Characteristic		Tested Specification			Data Sheet Specification			Units
				Min	Typ	Max	Min	Typ	Max	
D005	VBOR	BOR Voltage	BORV<1:0> = 0100	2.35	—	2.80	2.5	—	2.66	V
			BORV<1:0> = 0101	2.55	—	3.02	2.7	—	2.86	V
			BORV<1:0> = 0110	3.95	—	4.71	4.2	—	4.46	V
			BORV<1:0> = 0111	4.23	—	5.05	4.5	—	4.78	V

4. Module: LVD

The Low Voltage Detect module's selection ranges have changed. Table 2 shows the new specifications.

Work around

None.

Date Codes Pertaining To This Issue:

All.

Note:	When the manufacture date of a newer version of silicon is in production, the last date where this issue may occur will be specified.

TABLE 2: DC SPECIFICATION CHANGES FROM DATA SHEET

Param No.	Sym.	Characteristic		Tested Specification			Data Sheet Specification			Units
				Min	Typ	Max	Min	Typ	Max	
D420	V_{LVD}	LVD Voltage	LVV<3:0> = 0100	2.35	—	2.80	2.5	—	2.66	V
			LVV<3:0> = 0101	2.55	—	3.02	2.7	—	2.86	V
			LVV<3:0> = 0110	2.64	—	3.14	2.8	—	2.98	V
			LVV<3:0> = 0111	2.83	—	3.37	3.0	—	3.2	V
			LVV<3:0> = 1000	3.11	—	3.71	3.3	—	3.52	V
			LVV<3:0> = 1001	3.29	—	3.93	3.5	—	3.72	V
			LVV<3:0> = 1010	3.39	—	4.04	3.6	—	3.84	V
			LVV<3:0> = 1011	3.58	—	4.26	3.8	—	4.04	V
			LVV<3:0> = 1100	3.77	—	4.49	4.0	—	4.26	V
			LVV<3:0> = 1101	3.95	—	4.71	4.2	—	4.46	V
			LVV<3:0> = 1110	4.23	—	5.05	4.5	—	4.78	V

5. Module: Timer1

When Timer1 is running in Asynchronous mode and then disabled, data in the Timer1 register (TMR1) may become corrupted. Corruption occurs when the timer enable is turned off at the same instant that a ripple carry occurs in the timer module.

This issue only occurs in asynchronous operation. In synchronous operation, the relevant signals are latched with the CPU clock and the problem condition does not arise.

Work around

When Timer1 is configured to operate as an asynchronous counter, care must be taken that there is no incoming pulse while the module is being turned off. If an incoming pulse arrives while Timer1 is being turned off, the value of register TMR1 may become corrupted.

If an application requires that Timer1 be turned off, and if it is possible that Timer1 may receive an incoming pulse while being turned off, synchronize the external clock first by clearing the T1SYNC bit of register T1CON (T1CON<2>). Please note, however, that this may cause Timer1 to miss up to one count.

6. Module: A/D Converter

Exceptions have been observed in the differential linearity error specification (parameter A04), as listed in Table 15-9 of the Data Sheet.

No missing codes have been observed when using up to, and including, 11-bits of resolution. At 12-bits of resolution, up to four missing codes may occur. The missing codes will never be adjacent.

Work around

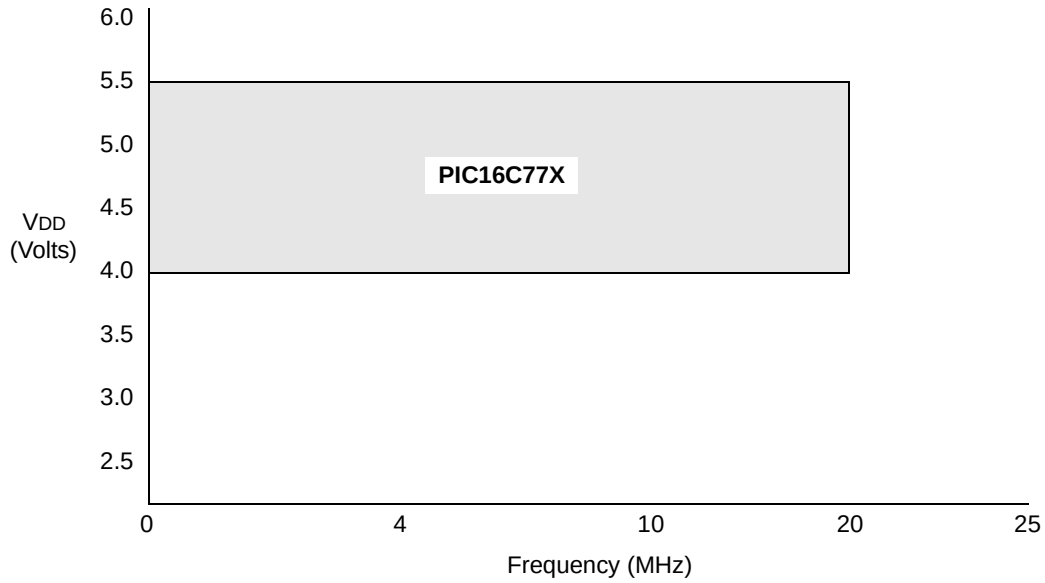
None.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS30275**A**), the following clarifications and corrections should be noted.

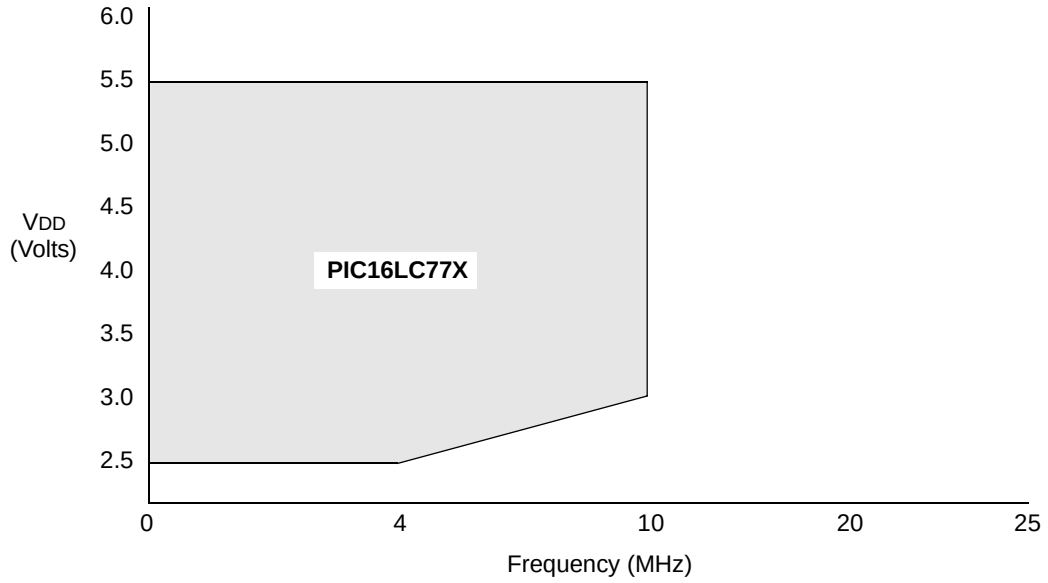
1. Table 15-1 in the Device Data Sheet (DS30275**A**) should be omitted. Figure 15-1 and Figure 15-2 below should be used to determine the operating voltages and frequencies for the devices.

FIGURE 15-1: PIC16C773/774 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +85°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

FIGURE 15-2: PIC16LC773/774 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +85°C



FMAX = (12.0 MHz/V) (VDDAPPMIN - 2.5V) + 4 MHz

Note 1: VDDAPPMIN is the minimum voltage of the PICmicro® device in the application.

2: FMAX has a maximum frequency of 10 MHz.

3: The shaded region indicates the permissible combinations of voltage and frequency.

2. The details of the new Product Identification System are given below. This information replaces the Product Identification System details given in the Device Data Sheet (DS30275**A**).

PIC16C774 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO. - X /XX XXX

Pattern:	QTP, SQTP, Code or Special Requirements	
Package:	JW	= Windowed CERDIP
	SO	= SOIC
	P	= PDIP
	SS	= SSOP
	L	= PLCC
	SP	= Skinny Plastic Dip
	PQ	= MQFP (Metric PQFP)
	PT	= TQFP (Thin Quad Flatpack)
Temperature Range:	-	= 0°C to +70°C
	I	= -40°C to +85°C
Device	PIC16C773	: VDD range 4.0V to 5.5V
	PIC16C773T	: VDD range 4.0V to 5.5V (Tape/Reel)
	PIC16LC773	: VDD range 2.5V to 5.5V
	PIC16LC773T	: VDD range 2.5V to 5.5V (Tape/Reel)
	PIC16C774	: VDD range 4.0V to 5.5V
	PIC16C774T	: VDD range 4.0V to 5.5V (Tape/Reel)
	PIC16LC774	: VDD range 2.5V to 5.5V
	PIC16LC774T	: VDD range 2.5V to 5.5V (Tape/Reel)

Examples

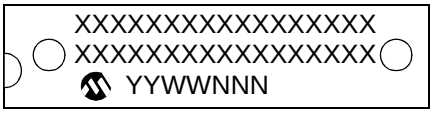
a) PIC16C774/P = Commercial Temp., PDIP Package, normal VDD limits.

*JW devices are UV erasable and can be programmed to any device configuration. JW devices meet the electrical requirement of each oscillator type (including LC devices).

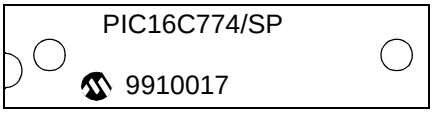
3. The PIC16C77X devices contain new package marking information. The package marking details provided below replace those given in Section 17 of the Device Data Sheet (DS30275**A**).

17.1 Package Marking Information

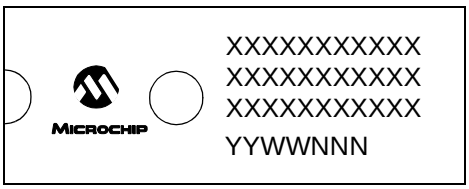
28-Lead PDIP (Skinny DIP)



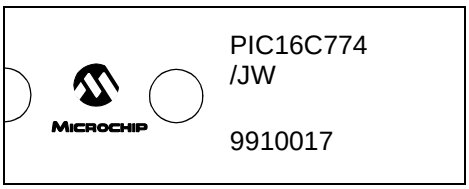
Example



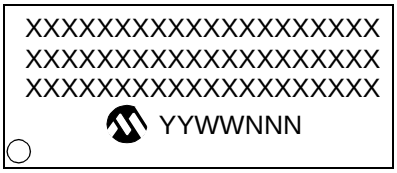
28-Lead CERDIP Windowed



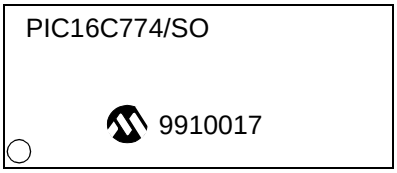
Example



28-Lead SOIC



Example



28-Lead SSOP

Example

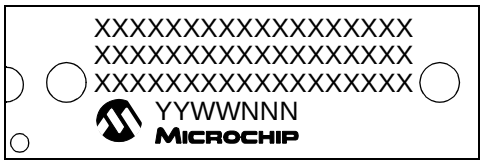
Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

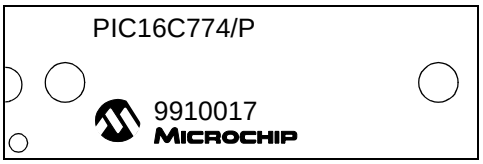
***** Standard OTP marking consists of Microchip part number, year code, week code and traceability code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

Package Marking Information (Cont'd)

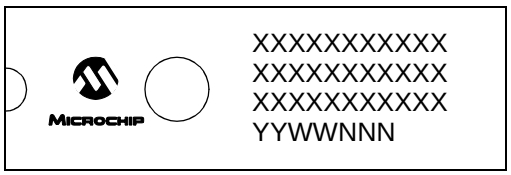
40-Lead PDIP



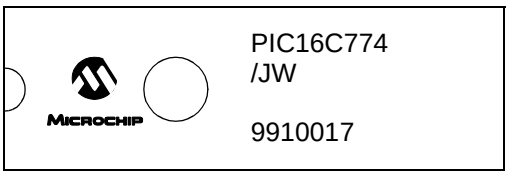
Example



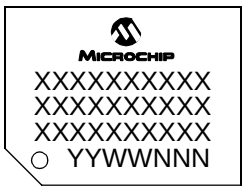
40-Lead CERDIP Windowed



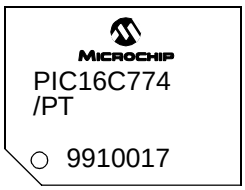
Example



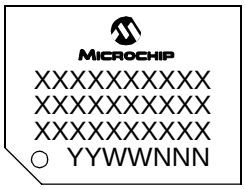
44-Lead TQFP



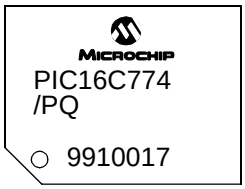
Example



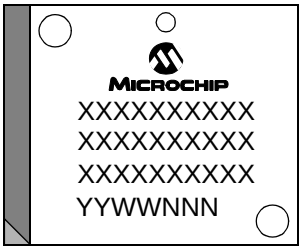
44-Lead MQFP



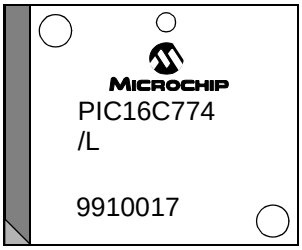
Example



44-Lead PLCC



Example



4. The A/D module differential current has been improved to the values shown in Table 3.

TABLE 3: DC SPECIFICATION CHANGES FROM DATA SHEET

Param No.	Sym.	Characteristic		New Specification			Data Sheet Specification			Units	Conditions
				Min	Typ	Max	Min	Typ	Max		
D026	ΔIAD	Module Differential Current **(Note 5)**									
		A/D Converter	PIC16**C**XXX	—	**10**	—	—	300	—	µA	VDD = 4.0V; A/D on, not converting
			PIC16**LC**XXX	—	**10**	—	—	300	—	µA	VDD = 3.0V; A/D on, not converting

Note 5: The Δ current is the additional current consumed when the peripheral is enabled. This current should be added to the base (IPD or IDD) current.

5. The Voltage Reference module line regulation specification has been changed to the values shown in Table 4. The new specification is shown in **bold**.

TABLE 4: DC SPECIFICATION CHANGES FROM DATA SHEET

Param No.	Sym.	Characteristic	New Specification			Data Sheet Specification			Units
			Min	Typ	Max	Min	Typ	Max	
D407	ΔVOUT/ΔVDD	Line Regulation	—	**1000**	—	—	—	50	µV/V

6. The Low Voltage Detect module supply current specification has been changed to the values shown in Table 5.

TABLE 5: DC SPECIFICATION CHANGES FROM DATA SHEET

Param No.	Sym.	Characteristic	New Specification			Data Sheet Specification			Units
			Min	Typ	Max	Min	Typ	Max	
D421	ΔILVD	LVD Supply Current	—	10	**TBD**	—	10	20	μA

7. The Brown-out Reset module supply current specification has been modified to the values shown in Table 6.

TABLE 6: DC SPECIFICATION CHANGES FROM DATA SHEET

Param No.	Sym.	Characteristic	New Specification			Data Sheet Specification			Units
			Min	Typ	Max	Min	Typ	Max	
D022A	ΔIBOR	Supply Current	—	10	**TBD**	—	10	20	μA

8. The A/D clock source bits (ADCS1:ADCS0) have had their operation modified. See Register 1 for a new definition of the ADCS1 and ADCS0 bits.

   Figure 1 shows how the TAD time is determined based upon the selection of the ADCS<1:0> bits and the source of VREF+ and VREF-. When VREF+ or VREF- comes from the internal voltage reference (VRH or VRL), then the required TAD time is increased by a factor of eight (see electrical specification parameter #130A).

   The clock source selected by the ADCS<1:0> bits is divided by eight when an internally generated reference voltage is used as reference to the A/D module. This automatically addresses the requirement for the TAD time, when the internal voltage reference is used as the A/D voltage reference.

Note:	Electrical specification parameter #130A is currently specified in the clarifications and corrections section of the Device Errata Sheet.

FIGURE 1: A/D CLOCK SOURCE BLOCK DIAGRAM

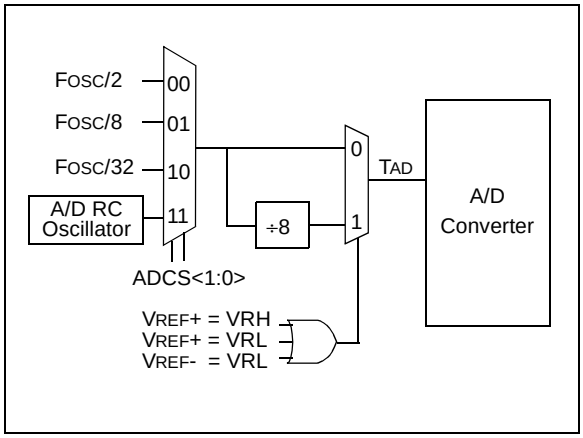


Table 7 shows the maximum device frequency depending on the A/D clock source selected.

REGISTER 1: A/D CONTROL REGISTER 0 (ADCON0)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	CHS3	ADON
bit 7							bit 0

bit 7-6 **ADCS<1:0>:** A/D Conversion Clock Select bits

ADCS<1:0>	**A/D Clock Source (TAD) =**	
	When VCFG<2:0> = 000, 001, 011 **or** 101	**When VCFG<2:0> =** 010, 100, 110 **or** 111
00	2 TOSC	16 TOSC
01	8 TOSC	64 TOSC
10	32 TOSC	256 TOSC
11	A/D RC (1 MHz max)	A/D RC (125 kHz max)

bit 5-0 No change to the operation of these bits

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

TABLE 7: MAXIMUM DEVICE FREQUENCY vs. A/D CLOCK SOURCE

ADCS<1:0>	A/D Clock Source (TAD)		Maximum Device Frequency
	When A/D Reference is selected as External Reference or Analog Supply TAD ≥ 1.6 µs	When A/D Reference is selected as Internal VRH or VRL TAD ≥ 12.8 µs	
00	2 TOSC	16 TOSC	1.25 MHz
01	8 TOSC	64 TOSC	5 MHz
10	32 TOSC	256 TOSC	20 MHz
11	A/D RC	A/D RC	— (1,3)

Note 1: The A/D RC source has a typical TAD time of 4 µs for VDD > 3.0V, but can vary between 2 µs and 6 µs.
2: The A/D RC source has a typical TAD time of 32 µs for VDD > 3.0V, but can vary between 16 µs and 48 µs.
3: When the device frequency is greater than 1 MHz, the A/D RC clock source is only recommended if the conversion will be performed during SLEEP.

9. The 12-bit A/D module requires some new timing specifications for the A/D clock period (minimum TAD time). These new specifications are for when the reference voltage for the A/D is selected as either the VRH or VRL reference voltage. The new specifications are shown in **bold** in Table 8.

TABLE 8: DC SPECIFICATION CHANGES FROM DATA SHEET

Parm No.	Sym	Characteristic		New Specification			Data Sheet Specification			Units	Condition
				Min	Typ	Max	Min	Typ	Max		
130	TAD	A/D Clock Period	Clock from FOSC	1.6	—	—	1.6	—	—	µs	VREF ≥ 2.5V
				TBD	—	—	TBD	—	—	µs	VREF full range
				12.8	—	—	N.A.	N.A.	N.A.	µs	VRH or VRL used as A/D reference voltage, VDD = 5.0V
			Clock from internal A/D RC oscillator ADCS<1:0> = 11	3.0	6.0	9.0	3.0	6.0	9.0	µs	VDD = 2.5V
				2.0	4.0	6.0	2.0	4.0	6.0	µs	VDD = 5.0V
				16	**32**	**48**	N.A.	N.A.	N.A.	µs	VRH or VRL used as A/D reference voltage, VDD = 5.0V

10. The output voltage specification in the DC Characteristics section has been modified to the values shown in Table 9. The new values are shown in **bold**.

TABLE 9: DC SPECIFICATION CHANGES FROM DATA SHEET

Param No.	Characteristic	Symbol	New Specification			Data Sheet Specification			Units
			Min	Typ	Max	Min	Typ	Max	
D400	Output Voltage	VRL	**1.9**	**2.048**	**2.2**	2.0	2.048	2.1	V
		VRH	4.0	**4.096**	**4.3**	—	4.096	4.2	V

REVISION HISTORY

Rev C Document (1/01)

Item 10 and Table 9, concerning output voltage specifications, were added.

Rev D Document (2/01)

Issues 5 (Timer1) and 6 (A/D Converter) were added (page 3).

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